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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/564,422
Filing Date: January 11, 2006
Appellant(s): DOOLEY ET AL.

Mark A. Wilson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/23/2009 appealing from the Office action mailed 4/28/2009

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 20010048713	Medlock et al.	12-2001
US 6657986	Laudel et al.	12-2003

US 5982811 Harrison et al. 11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 2, 4, 6 – 7, 9, 11 - 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Medlock (US 20010048713).

Regarding clam 1, Medlock discloses a method of correlating a sampled direct sequence spread spectrum signal with a locally provided replica signal containing a spreading code (Fig. 2A, input data 208 correlated with code sequence 210; Abstract, last 4 lines; Fig. 4A, block 4008; [0008]; wherein the local replica is the code sequence 210) the method comprising:

combining the bit or bits of at least two signal samples of the received signal to form a first word ([0029]; Fig. 2A, element 203a; wherein the combination of bits of the samples is the bit slices);

providing a second word containing bits corresponding to the replica signal ([0030]; Fig. 2A, element 202a; wherein the second word is formed from the local code sequence);

and executing one or more software based instructions to carry out word based hardwired operations to process the first and second words in order to obtain a correlation value (Fig. 2A; [0028] - [0029] which disclose the correlation is calculated; [0043], lines 7 – 9, which disclose word based operations, where the word based operations are the multiplications being performed in parallel).

Regarding clam 2, Medlock discloses the processing of the first and second words is done using hardwired circuitry ([0002], sentence starting with "Consequently, each application …").

Regarding clam 4, Medlock discloses a software based instruction is executed to form the first word ([0002], sentence starting with "Consequently, each application …").

Claims 6-7 and 9 are directed to apparatus of the same subject matter claimed in method/steps claims 1-2 and 4 respectively and therefore, are rejected as explained in the rejections of claims 1-2 and 4 above.

Regarding clam 11, Medlock discloses a direct sequence spread spectrum signal receiver comprising an antenna and an RF front-end including an analogue to digital converter for receiving spread spectrum signals and outputting corresponding signal samples; and a signal processor (Fig. 1, element 101, 103, 106a; [0023]).

Regarding clam 12, Medlock discloses a computer-readable storage medium having recorded thereon data containing instructions for performing a method according to claim 1 ([0058]; wherein the storage medium is the computer which has memory or the digital system memory).

Regarding clam 13, Medlock discloses a computer program comprising instructions for performing a method according to claim 1 ([0002] which disclose the application may utilize software i.e. computer program).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock (US 20010048713) in view of Laudel et al. (US 6,657,986).

Regarding claim 3, Medlock does not disclose the correlation is done using an XOR operation.

In the same field of endeavor, however, Laudel discloses the processing of the first and second words includes a word based XOR operation or its inverse and a summation of the results of that operation (column 4, lines 35 - 46).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the XOR method of calculating correlations, as taught by Laudel, in the system of Medlock because this would result in simplified hardware, as is well known in the art.

Claim 8 is directed to apparatus of the same subject matter claimed in method/steps claim 3 and therefore, is rejected as explained in the rejection of claim 3 above.

5. Claims 5, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock (US 20010048713) in view of Harrison et al. (US 5,982,811).

Regarding claim 5, Medlock does not disclose combining the sign bits, combining the magnitude bits and calculating the correlation value.

In the same field of endeavor, however, Harrison discloses each sample of the spread spectrum signal contains at least one magnitude bit and a sign bit; wherein the first word is formed by combining the magnitude bit or bits of at least two signal samples; wherein a third word is formed by combining the sign bit of at least two signal samples; and wherein one or more software based instructions are executed to process the first,

second and third words in order to obtain a correlation value (Fig. 8; column 15, lines 8 – 20; wherein the combination is done because of the columnar fashion arrangement of bits).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method as disclosed by Harrison, in the system of Medlock because this would result in simplified hardware, as disclosed by Harrison.

(10) Response to Argument

Argument: Appellant stated that:

(a) "In contrast to the language of the claim, Medlock does not disclose all of the limitations of the claim because Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value" (Appeal Brief 9/23/2009, page 6, 1st paragraph);

(b) …. herein, such discussion is merely presented in support of the argument that Medlock does not disclose word-based processing …. (Appeal Brief 9/23/2009, page 6, 2nd paragraph, lines 9 – 10);

(c) Thus, the description in Medlock of processing one chip at a time is at best analogous to processing one bit at a time (Appeal Brief 9/23/2009, page 6, 3rd paragraph, last 2 lines).

(d) Applicant's arguments on pages 7 – 9 are related to Applicant stating that Medlock does not disclose word based processing.

Response: Examiner respectfully disagrees.

Medlock (Fig. 2A) shows input data 208 and the locally generated code sequence 210 being fed to the fast searcher 102a. Fig. 3 shows one of the computing circuits 203a from Fig. 2A. The correlation of the input sequence and the code sequence is done by multiply circuit 304 and integrate circuit 306 in Fig. 3.

Applicant's claim 1 states that a first word is formed by combining the bit or bits of atleast two signal samples. In the case where a single bit is used, then each sample would essentially provide only 1 bit. Therefore, the correlation would be done by a word composed of 1 bit from several samples with the locally generated code sequence.

Medlock clearly states that several embodiments of his invention are possible ([0029]. In one embodiment, he says that different quantity of bit slices can be used . i.e multiple bits ([0029]). He further states that the multiply circuit has bit slices that contain multiply-logic device for parallel correlating operations on a chip-by-chip basis ([0042], lines 12 – 14; [0042] last 2 lines on page 4, right column; [0043], lines 7 – 9). Since parallel correlation is used it is clear that the word contains multiple bits and that these

are multiplied in parallel by the corresponding bits of the locally generated code sequence. Such a scheme would require several multipliers operating in parallel since all bits of the word are multiplied at the same time in parallel. This would constitute word based processing. In a bit based processing system, a bit from the input sequence would be multiplied by a bit from the local code sequence, then the next set of bits would be multiplied using the same multiplier, added to the fist product and so on. In this bit based scheme, only one multiplier would be needed and the multiplications would be done sequentially, not in parallel. As in well known to one of ordinary skill in the art, the parallel word based scheme requires more hardware but is faster than the sequential bit based scheme. Therefore, Examiner contends that Medlock discloses word based processing to do the processing as opposed t bit based processing.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Adolf DSouza

Assistant Examiner

AU 2611

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